Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for generating PN (pseudo noise) codes comprising:

a control unit for outputting a control signal for a normal state or a PN chip advance;

a plurality of multiplexers for outputting an output value of a next state for a normal operation or an output value of a following next state ($\vec{r}_{m+2}$) for a PN chip advance as an output signal in response to the control signal of said control unit;

a plurality of shift registers for outputting a PN chip code of a next state($\vec{r}_{m+1}$) or a following next state ($\vec{r}_{m+2}$) during one system clock time period in response to said outputs of the multiplexers, an input end of each of said shift registers being connected to an output end of each of said multiplexers,

wherein to obtain the output value of the following next state ($\vec{r}_{m+2}$) of ~~shifter~~ shift registers for one PN chip advance, the output values are determined based on the following equation:

$$\vec{r}_{m+2} = \lfloor r_{n,m+2}\ r_{n-1,m+2}\ \ldots\ldots\ r_{1,m+2}\ 0 \rfloor$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \textit{wherein } i \textit{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

wherein $\overrightarrow{r_m}$ is present state values of the ~~shifter~~ shift registers and $\overrightarrow{g_n}$ is parameter values of a generation polynomial.

2. (Previously Presented) The apparatus for generating PN codes according to claim 1, wherein said control unit further outputs a control signal for one PN chip retard; and wherein said multiplexers further output an output value of the related state for one PN chip retard.

3. (Currently Amended) A method of generating PN codes in a PN code generator comprising shift registers and using an nth order generation polynomial g(X)

$$g(X) = g_n X^n + g_{n-1} X^{n-1} + \ldots\ldots + g_1 X + 1,$$

the method comprising:

determining parameter values ($\overrightarrow{g_n}$) of the nth order generation polynomial by a first equation, wherein the first equation is

$$\vec{g} = [g_n g_{n-1} \quad \ldots\ldots \quad g_1 g_0]$$

$$g_i = \begin{cases} 1 & , i = n \\ 0 \text{ or } 1 & , 0 < i < n, \quad \text{wherein i is an [[interger]] integer;} \\ 1 & , [[i = n]] \; i = o \end{cases}$$

determining present states ($\vec{r}_m$) of shift registers of the PN code generator by a second equation, wherein the second equation is

$$\vec{r}_m = \lfloor r_{n,m} \quad r_{n-1,m} \quad \ldots\ldots r_{1,m} \quad r_{0,m} \rfloor$$

$$r_{i,m} = \begin{cases} 0 \text{ or } 1 & , 0 < i \le n, \quad \text{wherein i is an [[interger]] integer} \\ 0 & , i = 0 \end{cases}; \text{ and}$$

inputting state values into the ~~sift~~ shift registers for providing advanced states ($\vec{r}_{m+2}$) of the shift registers based on a third equation using the present states ($\vec{r}_m$) of the shift registers and the parameter values ($\vec{g}_n$), wherein the third equation is

$$\vec{r}_{m+2} = \lfloor r_{n,m+2} \; r_{n-1,m+2} \ldots\ldots r_{1,m+2} \; 0 \rfloor,$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) \} g_{i-1} \right], & 1 < i \le n, \textit{wherein i is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

4. (Currently Amended) The method for generating PN codes according to claim 3,

wherein[[:]] the PN generator uses a same system clock as ~~on~~ an output rate of the PN generator.

5. (Previously Presented) The method for generating PN codes according to claim 3, further comprising:

performing an operation for a PN chip retard for the LSSR by disabling external enable signals applied to each of the shift registers during one PN chip time period.

6-16. (Canceled).

17. (Currently Amended) A method of generating a PN code in a PN code generator comprising N number of ~~shifter~~ shift registers and using a same system clock as a PN chip rate, the method comprising:

calculating advanced state values of each shift register based on present state values of each ~~shifter~~ shift register; and

generating the PN code according to the advanced state values during one system clock time,

wherein the advanced state value is calculated based on the present state value using the following equations:

$$\vec{r}_{m+2} = \lfloor r_{n,m+2} r_{n-1,m+2} \ldots\ldots r_{1,m+2}\ 0 \rfloor$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \text{wherein } i \text{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

wherein $\vec{r}_{m+2}$ is the advanced state values of an nth shift registers, $\vec{r}_m$ is the present state values of the shift registers, and $\overrightarrow{g_n}$ is parameter values of a generation polynomial.

18. (Canceled)